A 60 μW Low-Power Low-Voltage Power Management Unit for a Self-Powered System based on Low-Cost Piezoelectric Powering Generators

J. Colomer-Farrarons*, P. Miribel-Català*,
*Electronics Department, Universitat de Barcelona
Instrumentaion and Communications Systems Lab. SIC
Barcelona, Spain
{jcolomer,pmiribel}@el.ub.es

A. Saiz-Vela*, J. Samitier*,**
**IBEC, Institut de Biotecnologia de Barcelona
μnanosystems Engineering for biomedical applications
Barcelona, Spain

Abstract— This paper presents the architecture of a novel implementation of an integrated self-powered system based on piezoelectric vibrations in a 0.13μm technology. The electromechanical transduction is performed by using a low-cost commercial piezoelectric, working at low frequencies, with voltages up to 2.5V. The system is conceived as a System In a Package (SiP). The full integrated system is adapted to work with low-voltage and low-power conditions. The full custom power management circuit is used to charge a storage capacitor (super capacitor), from which the stored energy will be used to power, by controlled cycles of discharge operation of a very low power wireless sensor node that could be used in heavy machinery monitoring. Each circuitry block of the power management circuitry is presented and discussed. The simulated studies are fully validated by experimental tests. The experimental consumption of the power management unit is 67μW, approach to the theoretical expected value of 60μW.

I. INTRODUCTION

Nowadays there is an enormous interest in renewable energy sources and its applications, in particular for high power levels [1] [2]. In the same way, there is an increasing interest in use external powering sources for small electronics systems, which is defined as energy harvesting [3]. This limited energy can be derived from different types of external ambient sources [4], like vibrations, heat, light or human activity, like in the classical work presented in [5], or in mobile electronics [6]. Interesting works show the design of self-powered systems based on MEMS micro-power sources, like an electromagnetic micro-power MEMS generators [7], variable capacitors, mini electromagnetic power generators or based on piezoelectric generators defining completely integrated sensor nodes [8].

The design of self-powered wireless networks [9] of distributed sensors, or portable devices to monitor the condition of motors, turbines, pumps and gear boxes in building automation, heating and ventilation control, burglar alarms, bio-applications [10] are in continuous development. There are also interesting examples of self-powered RF-ID to monitor the temperature working on ultra high bands [11] or for animal healthcare applications [12]. Vibration powered electronics devices have been applied in several commercial products, such as Seiko Kinetic wristwatch and smart tennis racquet [13].

The advances in semiconductor technologies related to the reduction of the transistor's size allow the industry to develop these new self-powered portable electronic devices that incorporate in a single SiP (System-in-Package) or SoC (System-on-Chip), a great variety of circuitry and functions. An example can be a wireless sensor network and biomedical electronics. The main problem with these new devices resides in the power supply system, which usually is based on a typical bulky battery solution often with a size much larger than the SiP or SoC.

The size, weight, finite energy lifetime and battery replacement are important drawbacks for those small and portable applications that need long lifetime energy supply systems [14]. In this way, new supply alternatives could be explored to remove or recharge the battery dependence. Therefore, a new trend in the energy sources for low power applications is growing rapidly in the last few years. This way consists in harvest the energy available in the environment to supply the enough power to the electronic applications instead of the use of battery technologies with short and finite amount of energy.

This work is focused on the development of a real power system based on PZT generators avoiding the use of typical DC-DC converters with external inductance widely used in piezoelectric energy scavenging applications [15-16].

The entire power management unit [17] or Power Conditioning Circuit (PCC) is presented in more detail, as well as the rectifier, the control module and a low power bandgap reference. These circuits have been designed in a 0.13μm technology from ST Microelectronics through the CMP-TIMA service.

In this work the conception of the Power Conditioning Circuit system is presented, based on the use of a piezoelectric generator. The full system is presented in section II. Section III explains the circuits as well as the piezoelectric power source. In section IV, simulations and experimental results are shown and discussed, followed by a conclusion in section V.

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II. System Conception

The system is conceived as a SiP (System-in-Package) where sensors, interface electronics, processing, wireless communications and power systems are combined in the same package. This work develops the powering part of the SiP based on a piezoelectric (PZT) as the main power source.

Fig. 1 presents the proposed architecture. The system is composed by an integrated AC/DC rectifier, an integrated switch transistor, an integrated Control Module, and an external super capacitor (SCapa).

The input based on a PZT generator supplies an AC voltage. This voltage is rectified by an AC/DC converter obtaining an unregulated DC voltage that is used to charge the super capacitor (SCapa).

A Control Module is added to the system to sense continuously the voltage at the super capacitor (SCapa) with two trigger values in order to control the PMOS switch, which is used to deliver the power to the load. The performance of the PCC is shown in Fig. 2. When the DC voltage at the SCapa reaches a maximum value (V_{max}) the Control Module switches on the Pmos and the energy stored in the SCapa is transferred to the load. At this point, the voltage at the capacitor starts to decrease (Discharging Phase) until a minimum voltage value (V_{min}). When the Control Module senses this minimum value the Pmos switch is deactivated and the voltage transfered from the capacitor to the load stops. At this point the voltage at the super capacitor charges again up to V_{max} defining the Recharge Phase. It must be stated that the rest of the SiP electronics must work between V_{max} and V_{min} voltages [16]. The time involved in the Start-Up and Recharge Phase until V_{max} varies in function of the power allowable by the generator and the value of the super capacitor. The Discharge Phase time depends on the load power consumption.

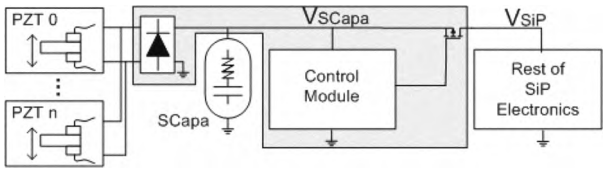

Figure 1. Proposed architecture for Self-Powered PCC (Pmos Switch).

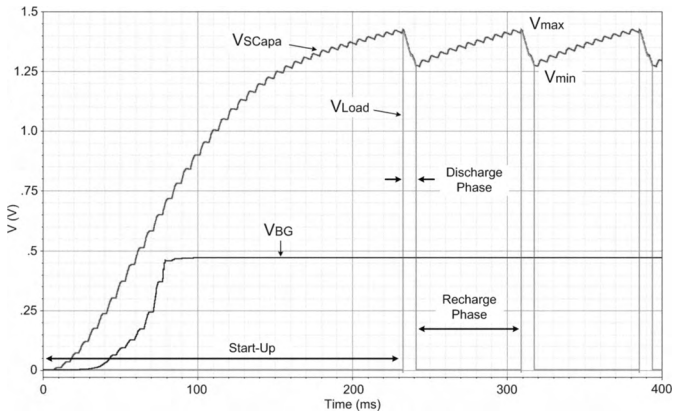

Figure 2. Performance of the prersented Power Conditioning Circuit (PCC).

III. Circuits

A. PZT Power Source

The experimental and simulated input is based on the Quick Pack QP20W from Midé Tech. A real and experimental Lumped Electrical Model compatible with Spectre software was developed [16] [18] to simulate the behavior of the PZT and verified in the Cadence environment. Using a frequency of 80Hz a current of 75µA and a peak voltage (V_{co}) of 1.2V with a load of 10kΩ is obtained.

To increase the current capability several PZT are used in parallel [15]. Currents of 120µA and 300µA are obtaining using 3 and 9 PZT in parallel respectively with a peak voltage of 1.2V@10kΩ. The piezoelectric open circuit voltage (V_{oc}) is 2.5V with an acceleration of 7m/s^2@80Hz. The maximum PZT transducer efficiency is achieve when $V_{co}=V_{oc}/2$ [19].

B. AC/DC Rectifier

Since the PZT generator supplies an AC voltage a rectification stage is needed. A full-wave NMOS rectifier was used, Fig.3a. Several simulations and Montecarlo analysis have been carried out obtaining an average efficiency for the rectifier around 70% and an average voltage drop against the transistor of 0.2V [17] [20] [21].

C. Control Module and Bandgap Reference Circuit

The architecture of the module is presented in Fig. 3c. The basic elements are two comparators, Fig. 3d, that sense continuously the voltage at the super capacitor (V_{SCapa}) and compare it with a reference voltage supplied by a band gap reference voltage, BG. Two resistive networks are used to adapt the level values of V_{SCapa} into the range defined by the band gap reference voltage. One of the comparators is prepared to sense when the voltage at the super capacitor reaches V_{max} and the other one is prepared to detect V_{min}. Also the comparators have been designed with a hysteresis of 20mV in order to define better the voltage detection points.

The band gap reference circuit used is based on a full MOSFET architecture [22] [23] because bipolar transistors are not implemented in the used technology. The final extracted voltage reference is 465mV for an input voltage supply from 1V to 2.5V. Its temperature coefficient is 100ppm/ºC, and its power consumption is 11µW. Fig. 3b presents the bandgap (BG) architecture. Both comparators share the same current source (CS) and bandgap to reduce the power consumption.

The signals generated by the comparators are used by a simple logical circuitry to generate the control signal for the PMOS switch and define the charge and discharge phases of the SiP, Fig. 1. The comparators and the digital logic are powered by the voltage at the super capacitor.

As it is commented previously the comparators are in charge of detecting the max and min voltages using the resistors network. In this way, several values of V_{max} and V_{min} can be selected using several values for the resistive networks. In this implementation, the control module is able to work with an integrated on-chip resistance network able to detect V_{max}=1.1V and V_{min} = 1.0V or with an external resistance allowing the system to work until a maximum voltage up to 2.3V.

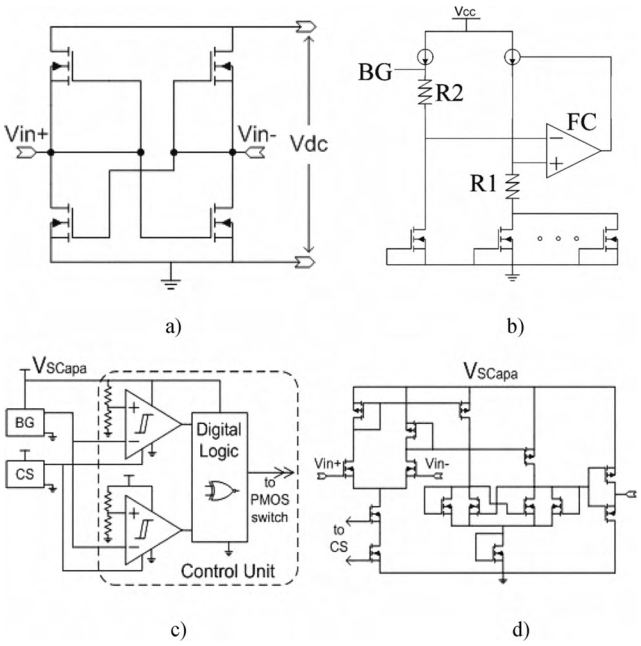

Figure 3. Nmos Rectifier, b)Bandgap circuit (BG), c) Control Module Architecture and d) Comparator Schematic.

IV. Simulation and Experimental Results

The circuit has been designed in 0.13µm Tech. by STMicroelectronics through CMP-TIMA. The circuit is shown in Fig. 4. The total size is 950µm x 550µm. To validate the circuit the experimental results have been compared with the simulated and some of them are presented in this section. The experimental setup is based on two Quick Pack piezoelectric, QP20W and QP40W [17]. Both transducers are mounted and clamped on an electromagnetic vibration shaker ET-132 Labworks Inc. The shaker is driven with the Pa-119 Labworks Inc. amplifier. A LC2442 laser by Keyence is used for the displacement measurements. Two Tektronix oscilloscopes TDS 2014 and TDS 714L are used to visualize the circuit and the Agilent Tech. N6705A DC Power Analyzer is used to verify the power consumption.

To verify the system an estimated power of 1.5mW has been assumed representing the consumption of the load. Also it is assumed that the power is consumed in pulses of 10ms.

The selected value of the capacitor is 47µF. A super capacitor or a high capacitor values are not used to avoid long simulations time. Using the previous values and taking into account that the energy transferred form the capacitor to the load is described by (1) where V_{max} and V_{min} are the defined max and min voltages values selected at the capacitor. With these values the total energy involved in the Discharge Phase is around 5µJ defining an average output current of 600µA. For this study 1.1V and 1.0V has been used as max and min voltages respectively. These values are obtained using the on-chip resistance network in the Control Module.

From the simulations several interesting values could be extracted. The start-up time is 230ms (Fig. 2), the time involved in the Discharge Phase is 8ms and in the Recharge

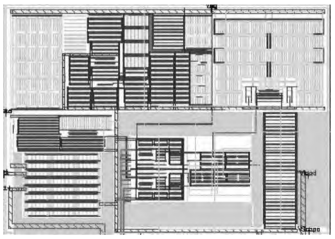

Figure 4. Final Die Implementation (950µm x 550µm).

$$\Delta E_{(J)} = \frac{1}{2} C_{SCapa} \left(V_{\max}\right)^2 - \frac{1}{2} C_{SCapa} \left(V_{\min}\right)^2 \qquad (1)$$

phase is 60ms (Fig. 5) for a typical case. The drop voltage across the PMOS switch is 11mV also for a typical case. Several Montecarlo simulations show that the drop voltage range can vary from 25mV to 3mV depending on the technological variation.

Fig. 6 presents the experimental start-up. The time involved in this phase is 250ms. The max voltage at the capacitor is 1.14V whereas V_{min} is 1.02V. The bandgap voltage is 438mV, also the same image presents the experimental Discharge and Recharge time of 10ms and 55ms respectively. The inset chart in Fig. 6 shows the 17mV of drop voltage across the switch.

The whole consumption of the electronics is 67µW. All experimental values are closed to the extracted simulated values and the system is fully validated. Successful test has been carried out using external resistors networks working with V_{max}=1.4 and V_{min}=1.2V and using several capacitor values for 1nF to 4700 µF.

As it is previously introduced in Section III.a the maximum mechanical to electrical efficiency is obtained when $V_{co}=V_{oc}/2$ where V_{oc} is the voltage generated by the piezo at no load condition and V_{co} is the voltage generated by the PZT with load connected to them. The transducer efficiency of the system is around 75-80% and it is independent of the capacitor value used as a SCapa thanks to the function of the control unit. In Fig. 7 it is possible to observe the relation between Voc and Vco. Also the discharge / recharge phase of the Scapa and the voltage transferred to the load could be observed.

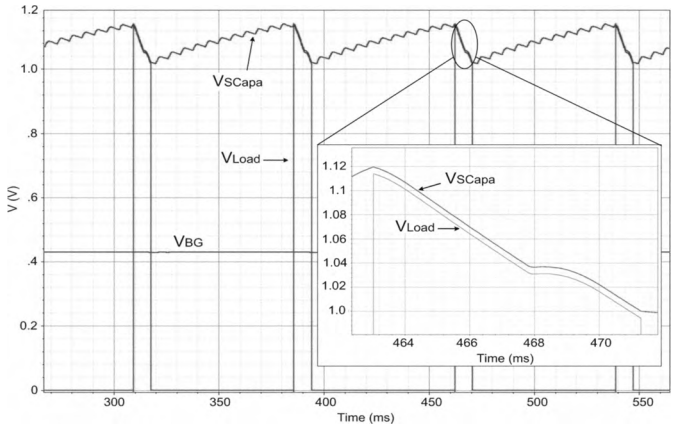

Figure 5. Steady State response and voltage drop across the Pmos Switch.

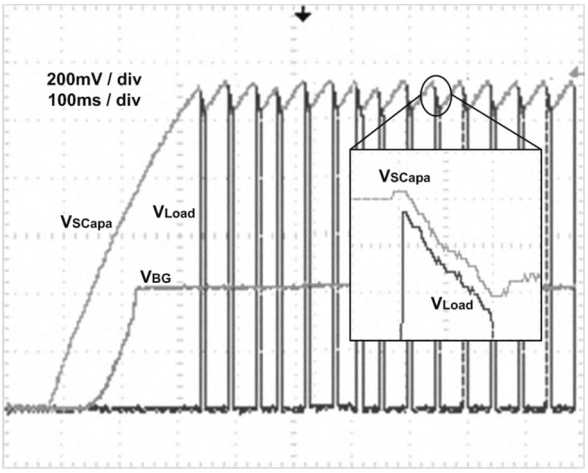

Figure 6. Experimental system Start-Up and Steady State response. Inset: voltage drop across the Pmos Switch.

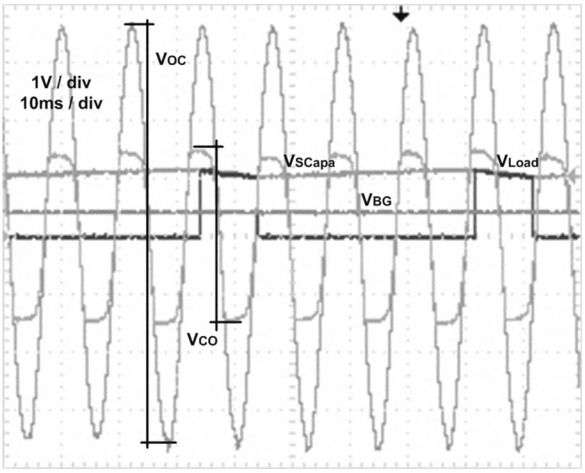

Figure 7. Experimentl Steady State response of the system and voltage drop across the Pmos Switch.

V. CONCLUSIONS

This paper presents a full custom power management circuitry for a self-powered system based on vibration energy scavenging, which is a low-cost piezoelectric commercial generator. The system has been designed using a low-power low-voltage commercial technology. The architecture of the proposed SiP is presented and each circuit block is described.

The experimental performance of the power management unit has been also presented and compared with the simulated values. The simulations are fully validated by experimental measurements. These results confirm the correct performance of the adopted architecture and demonstrated the ability of the architecture with respect the classical DC-DC converters and charge pumps.

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